

AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. **(Currently Amended)** An optical transceiver module, comprising:
a serial electrical interface with an electrical output port and an electrical input port;
a receive path comprising:

an optical input port for receiving a first optical signal from external to the transceiver module;

a receiver eye opener for retiming and reshaping a first serial electrical data stream based on the first optical signal, the receiver eye opener having an adaptive equalizer located in the receiver path and a clock and data recovery (CDR) unit coupled to transmit a recovered clock signal to the adaptive equalizer, wherein the CDR unit is located external to the receive path; and

the electrical output port of the serial electrical interface for transmitting the retimed and reshaped first serial electrical data stream to external to the transceiver module; and

a transmit path comprising:

an electrical input port of the serial electrical interface for receiving a second serial electrical data stream from external to the transceiver module;

a transmitter eye opener for retiming and reshaping the second serial electrical data stream; and

an optical output port for transmitting a second optical signal to external to the transceiver module, the second optical signal based on the retimed and reshaped second serial electrical data stream.

2. **(Original)** The transceiver module of claim 1 wherein the adaptive equalizer comprises a decision feedback equalizer.

3. **(Original)** The transceiver module of claim 1 wherein the adaptive equalizer comprises a feedforward filter.

4. **(Currently Amended)** The transceiver module of claim 1 wherein the ~~CDR unit recovers the receiver eye opener further comprises a clock and data recovery (CDR) unit for recovering a clock signal from the first serial electrical data stream and coupled to transmit the clock signal to the adaptive equalizer.~~

5. **(Currently Amended)** The transceiver module of claim 4 wherein the CDR unit is located external to the receive path and recovers the clock signal from the first serial electrical data stream before retiming and reshaping.

6. **(Currently Amended)** The transceiver module of claim 4 wherein the CDR unit is ~~located external to the receive path and~~ recovers the clock signal from the retimed and reshaped first serial electrical data stream.

7. **(Cancelled)**

8. **(Original)** The transceiver module of claim 1 further comprising:
a coefficient module coupled to receive the first serial electrical data stream and to transmit coefficients to the adaptive equalizer.

9. **(Original)** The transceiver module of claim 8 wherein the coefficients are based on autocorrelation functions of the first serial electrical data stream.

10. **(Original)** The transceiver module of claim 8 further comprising:
at least two analog correlation modules, each for calculating an autocorrelation function of the first serial electrical data stream, wherein the coefficients are based on the calculated autocorrelation functions.

11. **(Original)** The transceiver module of claim 8 wherein the coefficients are transmitted as analog signals from the coefficient module to the adaptive equalizer.

12. **(Original)** The transceiver module of claim 1 wherein the first serial electrical data stream has a data rate of approximately 10 Gb/s or faster.

13. **(Original)** The transceiver module of claim 1 wherein the transceiver module comprises an XFP (10-Gigabit Small Form Factor) –compliant transceiver module.

14. **(Original)** The transceiver module of claim 1 wherein the retimed and reshaped first serial electrical data stream comprises an XFI (10 Gb/s serial electrical interface)-compliant electrical data stream.

15. **(Original)** The transceiver module of claim 1 wherein the transmitter eye opener has an adaptive equalizer located in the transmit path.

16. **(Currently Amended)** An optical transceiver module, comprising:
a serial electrical interface with an electrical output port and an electrical input port;
a receive path comprising:

optical input means for receiving a first optical signal from the external to
the transceiver module;

receiver eye opener means for retiming and reshaping a first serial electrical data stream based on the first optical signal, the receiver eye opener means having an adaptive equalizer located in the receive path and means for transmitting a recovered clock signal to the adaptive equalizer, wherein the means for transmitting the recovered clock signal is located external to the receive path;
and

the electrical output means of the serial electrical interface for transmitting the retimed and reshaped first serial electrical data stream to external to the transceiver module; and

a transmit path comprising:

the electrical input means of the serial electrical interface for receiving a second serial electrical data stream from external to the transceiver module;

transmitter eye opener means for retiming and reshaping the second serial electrical data stream; and

optical output means for transmitting a second optical signal to external to the transceiver module, the second optical signal based on the retimed and reshaped second serial electrical data stream.

17. **(Currently Amended)** The transceiver module of claim 16 wherein the receiver-eye opener means further comprises means for recovering a clock signal is recovered from the first serial electrical data stream and for transmitting the clock signal to the adaptive equalizer.

18. **(Original)** The transceiver module of claim 16 further comprising:
- means for receiving the first serial electrical data stream, calculating coefficients in response to the first serial electrical data stream, and transmitting the coefficients to the adaptive equalizer.
19. **(Original)** The transceiver module of claim 18 wherein the coefficients are based on autocorrelation functions of the first serial electrical data stream.
20. **(Currently Amended)** An integrated circuit for use in a transceiver module, the integrated circuit comprising:
- a serial electrical interface with a first electrical output port and a first electrical input port;
- the first electrical input port being configured for receiving a first serial electrical data stream;
- receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream, the receiver eye opener circuitry including an adaptive equalizer and clock recovery circuitry coupled to transmit a recovered clock signal to the adaptive equalizer, wherein the clock recovery circuitry is located external to a data path from the first electrical input port to the first electrical output port; and

the first electrical output port being configured for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit.

21. **(Original)** The integrated circuit of claim 20 further comprising:

second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;

transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and

a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.

22. **(Original)** The integrated circuit of claim 20 wherein the adaptive equalizer comprises a decision feedback equalizer.

23. **(Original)** The integrated circuit of claim 20 wherein the adaptive equalizer comprises a feedforward filter.

24. **(Currently Amended)** The integrated circuit of claim 20 wherein the receiver-eye opener further comprises clock recovery circuitry recovers the for recovering a clock signal from the first serial electrical data stream ~~and coupled to transmit the clock signal to the adaptive equalizer.~~

25. **(Cancelled)**

26. **(Cancelled)**

27. **(Original)** The integrated circuit of claim 20 further comprising:

a coefficient module coupled to receive the first serial electrical data stream and
to transmit coefficients to the adaptive equalizer.

28. **(Original)** The integrated circuit of claim 27 wherein the coefficients are
based on autocorrelation functions of the first serial electrical data stream.

29. **(Original)** The integrated circuit of claim 27 further comprising:

at least two analog correlation modules, each for calculating an autocorrelation
function of the first serial electrical data stream, wherein the coefficients are based on the
calculated autocorrelation functions.

30. **(Original)** The integrated circuit of claim 27 wherein the coefficients are
transmitted as analog signals from the coefficient module to the adaptive equalizer.

31. **(Original)** The integrated circuit of claim 20 wherein the first serial electrical data stream has a data rate of approximately 10 Gb/s or faster.

32. **(Original)** The integrated circuit of claim 20 wherein the retimed and reshaped first serial electrical data stream comprises of XFI (10 Gb/s serial electrical interface)-compliant electrical data stream.

33. **(New)** The transceiver module of claim 1 wherein the adaptive equalizer is configured to adapt to changing temperature conditions.